**ECE 3380B lab 1: Automobile Tail-Light Control Unit**

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**1 Design Method**

**1.1 Combinational circuit**

A combinational circuit, called toggle, is first constructed that indicate the behavior of the eight lights. This circuit takes in 3 inputs (L, R, B) and generates 5 outputs. The first out llall ( left light all) will gives a signal 1 if inputs indicate all 4 left light needed to be on and 0 otherwise, the output rlall ( right light all) do the same thing but for all the right lights. rightflash gives a signal 1 if inputs indicate 4 right lights flash like Fig. 1 in Appendix A and leftflash gives a signal 1 if inputs indicate 4 left lights flash like Fig 2 in Appendix A, otherwise they give a 0 signal. AL give signal 1 when inputs indicate all light flash otherwise it will give a 0 signal

A inputs output relationship table is constructed based on table 1 in Appendix A:

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | L | R | B | lla | rlall | rightflash | leftflash | AL |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 2 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 3 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 4 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 5 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 6 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 7 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |

From the table llall, rlall, rightflash, leftflash, AL K-map made:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| llall |  | RB |  |  |  |
|  |  | 00 | 01 | 11 | 10 |
| L | 0 | 0 | 1 | 1 | 0 |
|  | 1 | 0 | 0 | 1 | 0 |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| rlall |  | RB |  |  |  |
|  |  | 00 | 01 | 11 | 10 |
| L | 0 | 0 | 1 | 0 | 0 |
|  | 1 | 0 | 1 | 1 | 0 |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| rightflash |  | RB |  |  |  |
|  |  | 00 | 01 | 11 | 10 |
| L | 0 | 0 | 0 | 1 | 1 |
|  | 1 | 0 | 0 | 0 | 0 |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| leftflash |  | RB |  |  |  |
|  |  | 00 | 01 | 11 | 10 |
| L | 0 | 0 | 0 | 0 | 0 |
|  | 1 | 1 | 1 | 0 | 0 |

Solving the K-map gives the output llall=BR+BL’, rlall=BR’+LB, rightflash=L’R and leftflash=LR’. AL is just min term 6 so AL=LRB’

**1.2 Sequential circuit**

Three sequential circuits needed to be designed to make the light flash like Fig. 1, Fig. 2 from Appendix A and all light flash.

**1.2.1 Sequential circuit for lights to flash light Fig. 1, Fig. 2 from Appendix A**

Beginning with the sequential circuit that makes the light flash like Fig. 1 Appendix A. This circuit is called flash1, it has 1 input X and for now it will be just the output leftflash of combinational circuit in 1.1. Whenever the input is 1, the circuit will moves to next state after it and give off apropriate 4 outputs represents 4 lights. If X is 0, the asynchonous preset and clear is use to force the circuit stay at initial state and set the 4 ouputs to be 0. Based on this information a state diagram is created:

Diagram, schematic

Description automatically generated

From the state diagram, a state table is created:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| PS | NS | | Output | |
| X=0 | X=1 | X=0 | X=1 |
| S0 | S0 | S1 | 0000 | 0000 |
| S1 | X | S2 | X | 1111 |
| S2 | X | S3 | X | 0111 |
| S3 | X | S4 | X | 0011 |
| S4 | X | S5 | X | 0001 |
| S5 | X | S0 | X | 1111 |

From the state table and diagram, it is noted that there are 5 states so in order to construct this circuit 3 D flip-flops are needed. The states are then represented as the outputs of 3 of these flip-flops, Q1Q2Q3. The convention that is used here are S0= 001, S1= 000, S2= 100, S3= 101, S4= 011, S5= 111, this weird convention is due to a mistake made in early state of development and only get corrected later but since this convention still follow the 3 rules and it was too late to change so I decided to keep it. The state table is then updated:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| PS | Q1­+ Q2+ Q3+ | | o3 o2 o1 o0 | |
| Q1 Q2 Q3 | X=0 | X=1 | X=0 | X=1 |
| 001 | 001 | 000 | 0000 | 0000 |
| 000 | X | 100 | X | 1111 |
| 100 | X | 101 | X | 0111 |
| 101 | X | 011 | X | 0011 |
| 011 | X | 111 | X | 0001 |
| 111 | X | 001 | X | 1111 |
| 010 | X | X | X | X |
| 110 | X | X | X | X |

From the table the K-maps of input of the three D flip-flop( Q1+, Q2+, Q3+) along with 4 output ( o0, o1, o2, o3) are made.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| o3 |  | X Q1 |  |  |  |
|  |  | 00 | 01 | 11 | 10 |
| Q2 Q3 | 00 | X | X | 0 | 1 |
|  | 01 | 0 | X | 0 | 0 |
|  | 11 | X | X | 1 | 0 |
|  | 10 | X | X | X | X |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| o2 |  | XQ1 |  |  |  |
|  |  | 00 | 01 | 11 | 10 |
| Q2Q3 | 00 | X | X | 1 | 1 |
|  | 01 | 0 | X | 0 | 0 |
|  | 11 | X | X | 1 | 0 |
|  | 10 | X | X | X | X |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| o1 |  | XQ1 |  |  |  |
|  |  | 00 | 01 | 11 | 10 |
| Q2Q3 | 00 | X | X | 1 | 1 |
|  | 01 | 0 | X | 1 | 0 |
|  | 11 | X | X | 1 | 0 |
|  | 10 | X | X | X | X |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| o0 |  | XQ1 |  |  |  |
|  |  | 00 | 01 | 11 | 10 |
| Q2Q3 | 00 | X | X | 1 | 1 |
|  | 01 | 0 | X | 1 | 0 |
|  | 11 | X | X | 1 | 1 |
|  | 10 | X | X | X | X |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Q1+ |  | XQ1 |  |  |  |
|  |  | 00 | 01 | 11 | 10 |
| Q2Q3 | 00 | X | X | 1 | 1 |
|  | 01 | X | X | 0 | 0 |
|  | 11 | X | X | 0 | 1 |
|  | 10 | X | X | X | X |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Q2+ |  | XQ1 |  |  |  |
|  |  | 00 | 01 | 11 | 10 |
| Q2Q3 | 00 | X | X |  |  |
|  | 01 | X | X | 1 |  |
|  | 11 | X | X |  | 1 |
|  | 10 | X | X | X | X |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Q3+ |  | XQ1 |  |  |  |
|  |  | 00 | 01 | 11 | 10 |
| Q2Q3 | 00 | X | X | 1 | 0 |
|  | 01 | X | X | 1 | 0 |
|  | 11 | X | X | 1 | 1 |
|  | 10 | X | X | X | X |

Solving the K-maps resulted in the function of 3 D flip-flops inputs: Q1+=Q3’+Q1’Q2, Q2+= Q1’Q2+Q1Q2’Q3, Q3+=Q1+Q2 (Fig. 1, Appendix C) and function of 4 outputs: o3=Q1’Q3’+Q1Q2, o2=Q3’+Q1Q2, o1=Q1+Q3’, o0=Q1+Q2+Q3’ (Fig. 2, Appendix C). The input X is wired to the clear of flip-flop 1, flip-flop 2 and wired to preset of flip-flop 3 to force state to stay at s0 when input is 0. Other preset and clear are wired to vcc.

Going through the same process to construct state diagram and table sequential circuit makes the lights flash like Fig. 2 Appendix A:

Diagram

Description automatically generated

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| PS | NS | | Output | |
| X=0 | X=1 | X=0 | X=1 |
| S0 | S0 | S1 | 0000 | 0000 |
| S1 | X | S2 | X | 1111 |
| S2 | X | S3 | X | 1110 |
| S3 | X | S4 | X | 1100 |
| S4 | X | S5 | X | 1000 |
| S5 | X | S0 | X | 1111 |

By comparing these diagram and table to the state diagram and table of flash1 sequential circuit, it is noted that both have the same number of state behavior and the outputs of these two situation is jus the opposite of each other, the outputs o0, o1, o2, o3 of flash1 are the outputs o3,o2,o1,o0 of sequential circuit implement Fig. 2 Appendix A respectively. Because of this, we could use 2 flash1 circuit to implements both Fig. 1 and Fig. 2 of Appendix A. In order to reduce the cost, we could use only 1 flash1 circuit to implement both of this situation by wire output A1 and A2 of the combinational circuit form 1.1 to an AND gate and the output will be X. There is a problem with this approach, if the L, R, B input of the combinational circuit from 1.1 go from L=1, R=0, B=don’t care to L=0, R=1, B= don’t care or vice versa, the flash lights will not start at all light off because technically the flash1 circuit never reset. To overcome this a sequential circuit was constructed called lrchange1bit that will detect this change and reset flash1 but if reset flash1 in this situation is not needed this circuit don’t need to implement to save cost.

The lrchange1bit circuit (Fig. 3 Appendix C) takes rightflash and leftflash output of combinational circuit from 1.1 as its inputs. rightflash and leftflash is also the inputs of 2 D flip-flop to hold information of rightflash and leftflash. This circuit detect a change of present state (Q1Q2) from 01 or 10 to 10 or 01 and give output of 1 otherwise it will stay at 0. Rightflash and leftf;ash can not be both 1 so whenever this happens Z output is don’t care. From this logic a state table is constructed:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Next state | | Present state | | Output |
| rightflash | leftlash | Q1 | Q2 | Z |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | X |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | X |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | X |
| 1 | 1 | 0 | 0 | X |
| 1 | 1 | 0 | 1 | X |
| 1 | 1 | 1 | 0 | X |
| 1 | 1 | 1 | 1 | X |

From the state table, a K-map is drawn:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Z |  | rightflash\*leftflash | | | |
|  |  | 00 | 01 | 11 | 10 |
| Q1Q2 | 00 | 0 | 0 | X | 0 |
|  | 01 | 0 | 0 | X | 1 |
|  | 11 | X | X | X | X |
|  | 10 | 0 | 1 | X | 0 |

Solving K-map result in Z= rightflash \*Q2+Q1 \*leftflash (Fig. 3 Appendix C). lrchange1bit was placed internally of flash1 because lrchange1bit takes in the same input as flash1, it need to use the same clock as flash1 in order to reset properly and it is wired to preset and clear of 3 flip-flops in flash1 instead of X. Output of lrchange1bit is wired to a NOT gate, lrchange1bit should just gives a 0 when it detected a reset is needed but when making this I may be forget that clear and preset of flip-flop is active low. The output of that NOT gate is wired to a AND along the output of rightflash AND leftflash. And the output of that AND is wired to clear of flip-flop 1, clear of flip-flop 2 and preset of flip-flop 3. The rest of clear and preset is still wire to vcc(Fig. 4 Appendix C). There is also a testing output of lrchange1bit called al in testbench Fig. 1.

**1.2.2 Sequential circuit for all light flash**

This is a simple design, it is just a sequential circuit that alternate between giving output of 1 or 0 each cycle when it is active. All is needed is just a D flip-flop that has input Q+ as Q’ AND with the output alf of combinational circuit from 1.1, alf serves as enable and it also wired to clear of that flip-flop to reset it when it inactive. Q’ AND with the output alf is also the output of this circuit that will be wired to light to make them flash. (Middle top of Fig. 1 Appendix E).

**1.2.3 Clock**

A 1Hz clock can be made by using Quartus IP catalog. An LPM\_COUNTER is used to keep track of 50,000,000 clock cycle, its input is the 50 MHz FPGA clocks. The output of counter is then wired using bus connection to input LPM\_COMPARE to check the value is greater than the half way point or 25,000,000. And the output of LPM\_COMPARE is the output of the clock. (Appendix D)

**1.3 The complete circuit (Appendix E)**

Three input l,r,b is wired to “toggle” form 1.1. the output of llall of it control all light on so it is as simple as wired them to all 4 left light outputs but since it is not the only one control left light, it will be the one of input of 4 OR gate that the output of those OR gates are the 4 left lights. Do the same thing for rlall but or the 4 right lights. The outputs sequential circuit control all light flash in 1.2.2 is also wired to the 8 OR gate that output are the 4 left lights and 4 right lights. Leftflash and rightflash output of “toggle” are input of flash1. The output o3 of flash1 is wired with leftflash as inputs of AND. The output of AND gate will be one of input of OR gate that has output as left light 0 (l0o). Carrying out the same procedure for the other 3 output of flash1 with o2 correspond to l1o, o1 correspond to l2o and o0 correspond to l3o. For wiring flash1 output to control right light, output o3 of flash1 is wired with rightflash as inputs of AND. The output of AND gate will be one of input of OR gate that has output as right light 3 (r30). Carrying out the same procedure for the other 3 output of flash1 with o2 correspond to r2o, o1 correspond to r1o and o0 correspond to r0o. The clock circuit takes in 50MHz FPGA clock and its output is wired to clock input of flash1 and sequential circuit control all light flash in 1.2.2.

**2. Testbench**

Using time period of 500ns with a 10ns time period, the following functional simulation shows the eight possible outputs of the circuit. The timing simulation only supported by Cyclone IV and Stratix® IV FPGAs and the DE-10 standard using in this lab is Cyclone V so the timing simulation is identical to the functional simuation.

Fig. 1: Functional simulation

Timeline

Description automatically generated with medium confidence

Fig 2: Timing simulation

A picture containing application

Description automatically generated

**A Appendix**

**Appendix A: Lab handout**

Table

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**Appendix B: Combinational circuit**

Fig.1: Schematic of combinational circuit “toggle”

Diagram, schematic

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**Appendix C: Sequential circuit flash1**

Fig 1: Schematic of left-half of flash1 or D flip-flop portion

Diagram, schematic

Description automatically generated

Fig. 2: Output of flash1

Diagram, schematic

Description automatically generated

Fig. 3: Schematic of lrchange1bit

Diagram, schematic

Description automatically generated

Fig. 4: Complete schematic of flash1

Diagram, schematic

Description automatically generated

**Appendix D: Clock circuit**

Fig. 1: Schematic of clock circuit

Diagram

Description automatically generated

**Appendix E: Complete circuit**

Fig. 1: Schematic of complete circuit

Diagram, schematic

Description automatically generated